

Low-Cost Receiver with Microcontroller-Based Demodulation

Signal Processing with Microcontrollers Beyond their Specs

Graduate



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Introduction: In many applications, the use of increasingly powerful streamlined off-the-shelf components is becoming an interesting and cost-effective alternative to the traditional implementations. One such case is the sampling and demodulation of HF signals with the use of microcontrollers. Shifting more functionality into the microcontroller may provide benefits in system cost, size and complexity, enabling new designs to be a lot cheaper while keeping performance high.

Approach: To assess the feasibility of using a microcontroller for the sampling and demodulation task of HF signals, the capabilities of STM32G4 and STM32H7 controllers were investigated and multiple system concepts were proposed. The approach of relying exclusively on the internal functionality of a STM32H723 was further evaluated by quantifying performance in the frequency domain first on an official evaluation board and then on a custom hardware prototype. This process included understanding key mechanisms like aperture jitter and phase noise that are responsible for a rising noise floor as well as modulation and spurious effects. For this task, information on the relevant theory and design constraints was compiled, measurement scripts were written and the hardware prototype was developed and assembled.

Result: The measurements confirm that by complying with various design constraints and optimizations, the controller can be used beyond its specified design to perform microcontroller-based subsampling of a HF signal with decent performance. For an oversampled HF carrier at 15.125MHz, a SNR of 68dB, equivalent to 11 effective number of bits and a SFDR of 73dB was achieved within a 30kHz bandwidth as shown in Fig. 2.

ENOB vs. Amplitude relation due to the ADC aperture jitter.
Own presentation

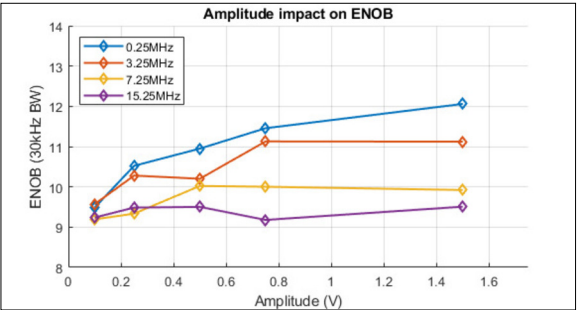


Fig.2: Frequency spectrum of the subsampled HF carrier.
Own presentation

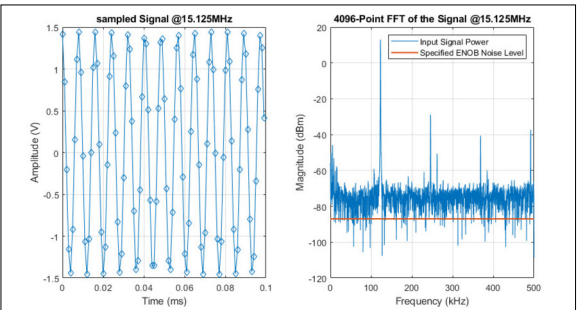
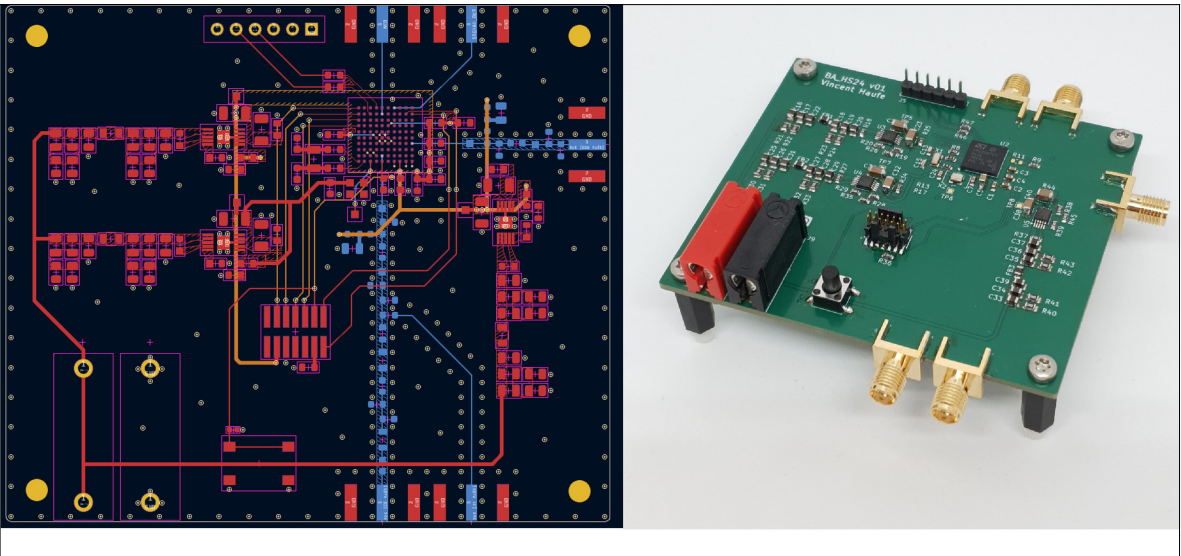


Fig.3: Hardware Prototype.
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Subject Area

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