Transceiver-based Time-to-Digital Converter

Graduate

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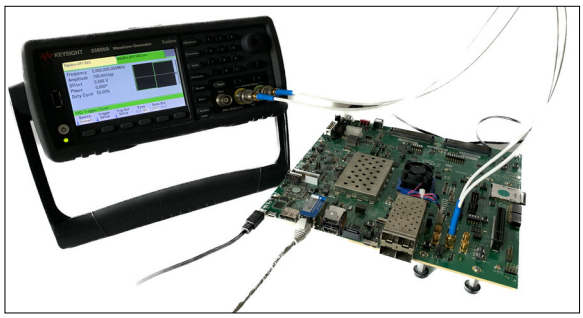
Introduction: Precise measurement of small time intervals is crucial in various fields, including fluorescence-lifetime imaging microscopy, which investigates physiological processes on a cellular scale. This technique requires a Time-to-Digital Converter (TDC) to convert time intervals into digital signals. Traditional TDCs, such as those based on counters, delay lines, and ADCs, often encounter challenges like high complexity, resource intensity, and latency.
This thesis introduces a novel approach to TDC design, utilising a Gigabit Transceiver High-performance (GTH) transceiver integrated into an FPGA. Typically employed for high-speed data transmission, a GTH transceiver can sample at 16.375 GHz , offering a time resolution of approximately 61 ps. While this resolution is not as fine as some existing TDCs, the GTH-based TDC provides multi-hit capability and resource efficiency, making it suitable for applications requiring high reliability and simple implementation.

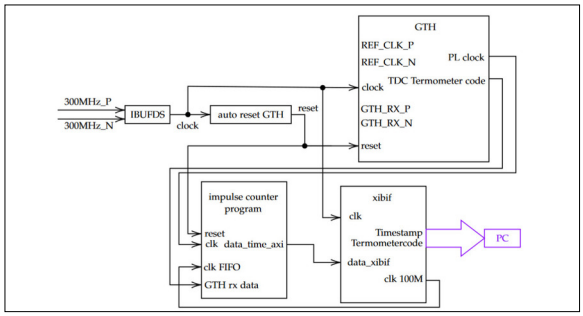
Result: Experimental results demonstrate that the GTH-based TDC can measure a 10 ns pulse with a standard deviation of around 70 ps . For a 100 ns pulse, a standard deviation of under 61 ps was achieved, corresponding to an error of 1 to 2 quantisations. Compared to other TDCs, which may offer higher accuracy, an error of ±2 quantisations is satisfactory. Given the nature of the process being discrete a standard deviation of less could be realistic

Conclusion: Further research and potentially using different hardware could enhance the accuracy and reliability of this TDC. The current ZCU102 board imposes limitations on adjusting the GTH transceivers, which are not typically designed for non-data transmission applications. Nonetheless, a TDC implemented without additional hardware revolutionises high-resolution time measurements, making them accessible for various applications, including faster and more efficient fluorescence-lifetime measurements, as there is no latency.

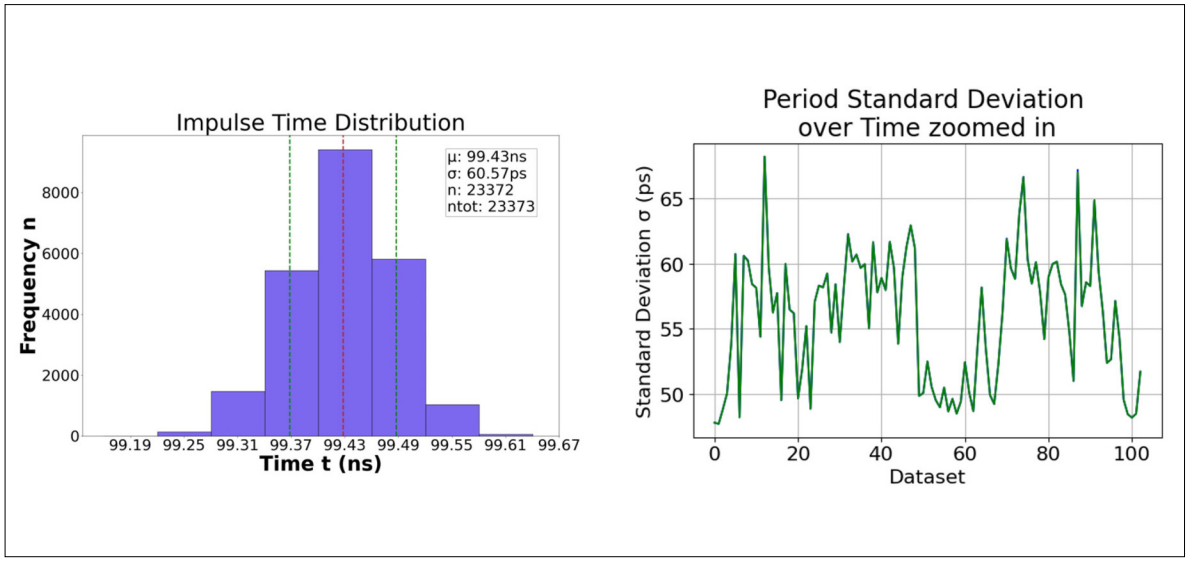
Hardware setup for the TDC
Own presentment



A rough diagram of how the TDC embedded in the FPGA
Own presentment



Graphs of the GTH results given a 5MHz input signal
Own presentment



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Subject Area
Microelectronics

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