Wave Union TDC

Improving Sub-Clock time measurement by using multiple Signal Edges and the Decomposition Scheme

Graduate

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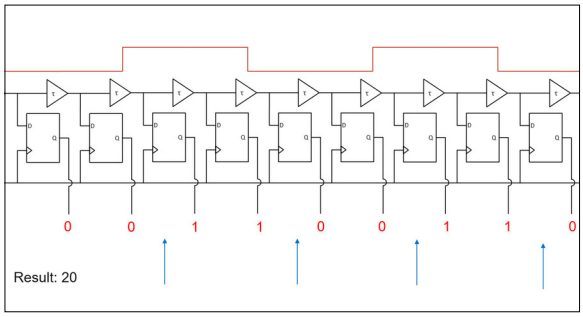
Introduction: High accuracy time measurements in the order of picoseconds, required in Fluorescence Lifetime Microscopy and Time of Flight (ToF) applications can be achieved with Time to Digital Converters (TDC). Classical timing methods require high-frequency clock counters which are impractical for such small time units, as running at clock speeds in the upper gigahertz range introduces additional high-frequency effects. A possible solution is to produce an Application-Specific Integrated Circuit (ASIC), but the cost and development time for one specific use case is enormous. Instead, the hardware of a Field Programmable Gate Array (FPGA) can be used to achieve sub-clock time resolutions. Wave Union TDCs (WU TDC) can be superior to other architectures in terms of performance. Unlike classic TDCs, they use multiple edges to measure how far a signal has travelled through a series of delay elements during a clock cycle. With the desired improvement in time resolution, new problems arise which are not obvious but must be considered when designing this type of TDC. A possible solution with all its components is presented and explained in this work.

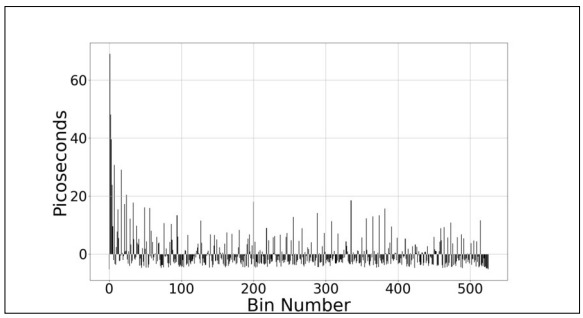
Approach: Several designs of WU TDCs have been published. After a thorough literature study on WU TDCs, the Decomposition Encoding Scheme was chosen. This was combined with a WU Launcher with a finite number of transitions, since a very large number of transitions does not improve the resolution significantly. This encoding scheme has an integrated bubble filter and its functionality is easy to comprehend. For this type of TDC, two parameters are of great importance: the maximum bubble depth, which greatly affects the structure of the encoder and launcher, and the propagation speed of an edge within one clock cycle. Appropriate measurements revealed the specific design parameters of the FPGA at hand, which was an Artix-7 embedded in a Xilinx Zynq-7020. According to these characteristics, the WU launcher and the encoder were implemented step by step. As this TDC operates at a system frequency of 360 MHz, meeting the timing requirements proved to be the biggest challenge. As FPGAs were designed for synchronous operation, the handling of asynchronous signals presented additional challanges.

Result: Measurements revealed that the performance of the TDC is highly dependent on the hardware used. Several implementations on different Zynq-7020s resulted in varying time resolutions. The best resolution of 5.3 ps was achieved with a four-edge WU TDC. A TDC with two edges achieved a resolution of 10.9 ps. The precision was specified by conducting a reference measurement, where a specific time value is measured multiple times, resulting in a Gaussian curve. The presicion was specified as 14.9 ps and 13.5 ps for two and four edge TDCs respectively. Higher numbers of edges could not be measured due to timing issues of the design. Of the designs that could be measured, the resolution and the percision were determined and compared to a Tapped Delay Line TDC (TDL TDC). This thesis proves that the concept of WU TDCs using the decomposition scheme achieve better resolutions than the previous TDL architecture. As previously published papers did not discuss the whole design in detail and focused more on the results, this work builds a foundation for future undertakings by explaining all design steps in detail. Key performance limiting factors have been identified and described so that this design can be further improved in the future.

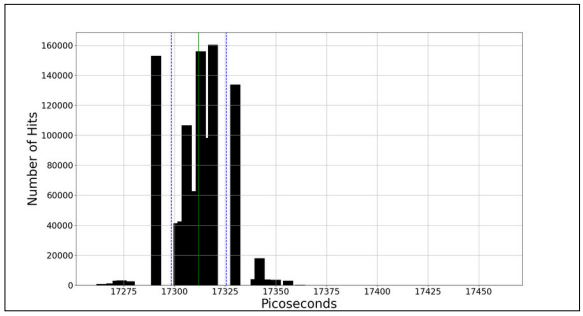
Schematic of a Wave Union within a delay chain sampled with registers.
Own presentment



DNL of a Wave Union TDC with four Edges
Own presentment



Gaussian curve resulting from multiple reference measurements with a standard deviation of 13.5ps.
Own presentment



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