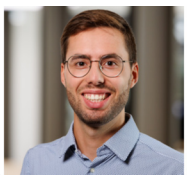
UWB FMCW Radar Frontend Design

A Sub-10GHz FMCW Radar Analog Frontend Design in a 22nm CMOS FDSOI IC Process

Graduate



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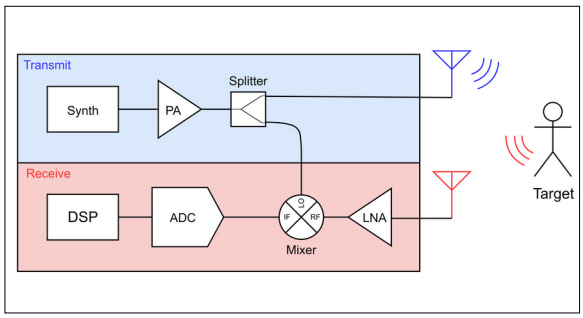
Introduction: Radar sensors offer several advantages over camera-based systems, including enhanced privacy, low power consumption, reliable performance in harsh environments, and immunity to lighting conditions. CSEM is exploring the development of UWB (6–10GHz) FMCW Radar-on-chip frontends as a complement to its ongoing 60GHz and 240GHz radar-on-chip initiatives. Radar sensors operating below 10GHz provide robust sensing capabilities with significantly lower power consumption. These characteristics make them particularly well-suited for applications such as presence detection and tracking, where ultra-high range resolution is not required but ultra-low power operation is critical.

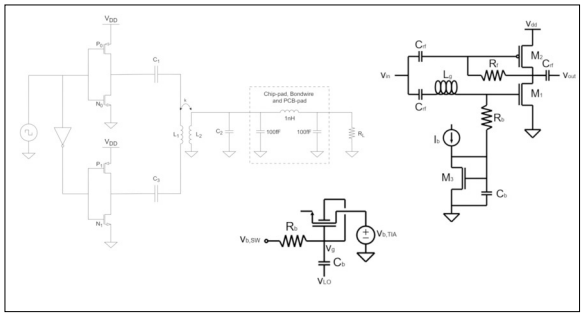
Approach / Technology: The working principle of an FMCW radar with its parameters and tradeoffs were reviewed, along with its main components, such as PAs, LNAs and mixers. The system requirements were determined, from which the block requirements were derived. Recent publications on the main components were reviewed, tested and compared for their performance in accordance to the requirements, from which the architecture for the receiver chain was determined. After investigating effects occurring at RF, as well as noise and nonlinearity effects in deep-submicron devices, the size and biasing were optimized for the best performance. The circuits were analyzed, developed and continuously optimized in a 22nm FDSOI IC process, using the real active and passive devices. Transformer and inductor coils were developed to complement the circuits. The RF cores were transferred to layout, where the parasitics were extracted and the circuits optimized.

Result: A Class-D PA using a transformer-based matching network was developed achieving an output power of 10.5dBm with a PAE of 50% across a frequency range from 7GHz to 9GHz. A switch-based current-mode passive mixer was developed for optimal receiver linearity. A single-stage inverter-based LNTA with a pole-splitting technique was developed. At the center frequency, this receiver chain achieved an IRL of -11.9dB, a NF of 13.1dB, a gain of 31.8dB with sufficient linearity measures for IIP3 and P1dB of 3.5dBm and -8.3dBm respectively.

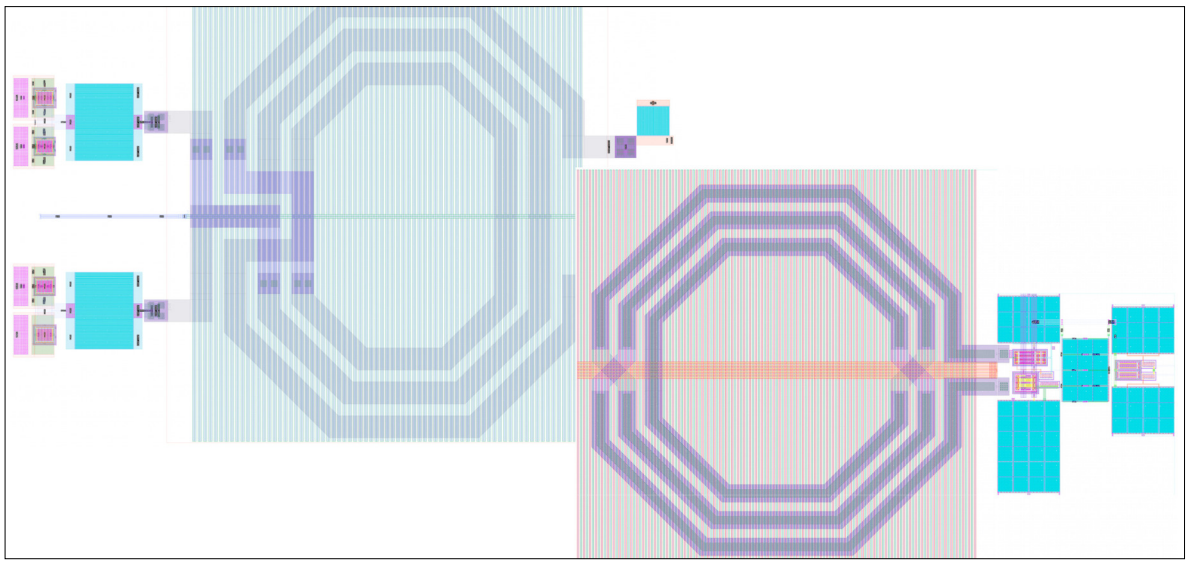
Analog Frontend Block Schematic of an FMCW Radar
Own presentment



Schematics of PA, LNTA and mixer
Own presentment



IC Layout of the RF Core
Own presentment



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